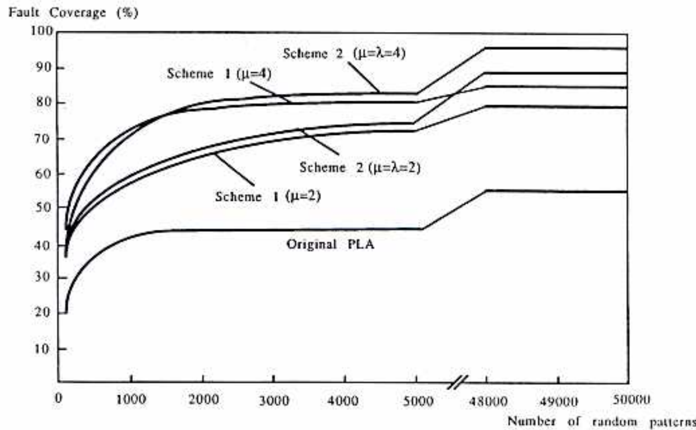

Fig. 6. Random-pattern test coverage curves for PLA 2.

modified PLA of scheme 2 achieved a 95.4 percent fault coverage with 50 000 patterns when $\mu = \lambda = 4$. Therefore scheme 2 with $\mu = \lambda = 4$ is the best among them for achieving a high fault coverage.

V. Conclusion

We have proposed a design of random-pattern testable PLA's. The proposed design is realized with very low area overhead: 0.84 percent through 15.25 percent for eight benchmark PLA's. We have also presented experimental results to show that the fault coverage can be significantly enhanced; for example, a 54.6 percent fault coverage with 50 000 pseudorandom patterns of an original PLA can be enhanced to 95.4 percent after modification of the PLA with 5.35 percent additional logic. The experimental results show that the proposed approach achieved almost 100 percent fault coverage in pseudorandom testing with very low area overhead for all eight benchmark PLA's.

Acknowledgment

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Schwarz–Christoffel Transformation for the Simulation of Two-Dimensional Capacitance

Ç. K. KOÇ and P. F. ORDUNG

***Abstract*—An inherent problem in the use of simulators for the determination of capacitance in VLSI circuits is the verification of the reliability of the simulation. The problem is due to the numerical approximations made in order to achieve a versatile simulation. The Schwarz–Christoffel transformation provides theoretically exact simulation of a limited class of problems consisting of two odd shaped conductors embedded in a uniform dielectric. We propose that the Schwarz–Christoffel technique can be used to calibrate simulators designed for more general problems.**

I. Introduction

Estimating parasitic capacitance of VLSI buses is a crucial step in computing circuit delay, particularly as packing density increases and conductor spacings decrease [5]. A great deal of effort has been spent in designing simulators which take the cross section geometry of the conductor–dielectric system as input, and compute the capacitance per unit length between the metal lines [2], [3].

The numerical methods to estimate the capacitance are usually CPU intensive, and thus prohibitive for VLSI layouts. Another solution is to find geometry-dependent approximate formulas which require short run times and a modest amount of memory [1]. An inherent problem in using simulators to estimate the parasitic capacitance is the difficulty of determining the reliability of the predicted capacitance values. The reason for this is that all methods in one way or another involve approximations which are difficult to evaluate.

The Schwarz–Christoffel conformal mapping technique, on the other hand, does not require *a priori* approximations. As long as the computations can be performed free of round-off error, the computed value would be the exact capacitance of the conductor–dielectric system. The Schwarz–Christoffel mapping technique provides theoretically exact estimates for a limited class of problems, which can be used to check the reliability of simulators designed for more general problems.

II. Schwarz–Christoffel Transformation

In this section, we show the application of the Schwarz–Christoffel conformal mapping technique for a class of capacitance problems. We consider a pair of conductors which exhibit symmetry

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Ç. K. Koç is with the Department of Electrical Engineering, University of Houston, Houston, TX 77204.
P. F. Ordung is with the Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106.

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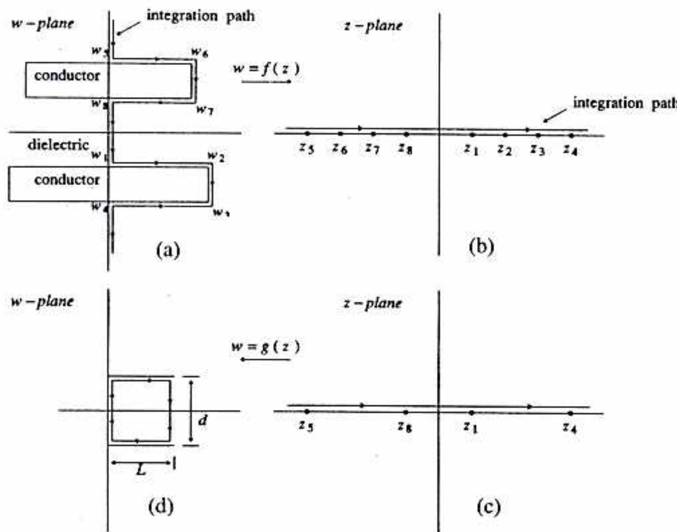

Fig. 1. The Schwarz-Christoffel mapping technique.

about the vertical axis, as in Fig. 1(a). We assume that the conductors are defined in the complex w plane. The Schwarz-Christoffel problem is to find an integral transformation for the z plane such that an integration around the contour in the direction of the arrow generates the contour in the w plane as shown in Fig. 1(a) and (b). The contour follows the path generated by the surface of the conductors and the imaginary axis, and finally closes with the circle at infinity. The Schwarz-Christoffel transformation is expressed as an integral:

$$w = f(z) = A \int_0^z \prod_{k=1}^{n} (\zeta - z_k)^{-\beta_k} \, d\zeta.$$

There is a one-to-one correspondence between the singularities in the z plane and the corners in the w plane. The exponents β_k are associated with the angles at the corners α_k in the w plane. They satisfy the following:

$$\beta_k = \frac{\alpha_k}{\pi} \quad \text{and} \quad \sum_{k=1}^{n} \beta_k = 2 \tag{2}$$

where α_k is the exterior angle at the kth corner [6]. The value of the exponent determines the angle of rotation of the corner generated as one maps through the corresponding singularity z_k.

The Schwarz-Christoffel mapping problem is defined as the determination of the constant A and the location of the values of z_k (which are called the *accessory parameters* [6]) such that the generated mapping properly encloses the conductors in Fig. 1(a). Once the mapping problem has been solved, it is very easy to compute the exact capacitance between the conductors. This is based on the fact that contours within the region in the w plane must map (on a one-to-one correspondence basis) to contours in the z plane, and all angles must be conformally preserved in the mapping. If we define another mapping from the z plane back to the w plane by using only the singularities at the outer points (as shown in Fig. 1(c)) and the following integral,

$$w = \int_0^z (\zeta - z_1)^{\gamma_1} (\zeta - z_2)^{\gamma_2} (\zeta - z_3)^{\gamma_3} (\zeta - z_4)^{\gamma_4} \, d\zeta \tag{3}$$

where

$$\gamma_1 = \gamma_2 = \gamma_3 = \gamma_4 = -\tfrac{1}{2}$$

then the contour generated in the w plane will be the rectangle shown in Fig. 1(d). The top and bottom sides in Fig. 1(d) now correspond to the conductor plates in Fig. 1(a), and therefore have equipotential. Furthermore, the field produced is confined to the interior of the rectangle. Thus the rectangle in Fig. 1(d) corresponds to an ideal capacitor equivalent to the plates shown in Fig. 1(a). The exact capacitance (per unit length) can be computed as

$$C = 2 \frac{L}{d} \kappa \epsilon_0 \quad \text{(F/m)} \tag{4}$$

where κ is the dielectric constant of the insulating material, and $\epsilon_0 = 8.85 \times 10^{-12}$ (F/m) is the permittivity constant of vacuum.

III. Numerical Simulation

The application of the Schwarz-Christoffel conformal mapping technique to determine capacitance was pointed out by Palmer in an expository paper [4]. Palmer applied this technique to compute the capacitance of a parallel-plate air capacitor without neglecting the fringing of the flux. Since the plates are assumed to have *zero thickness*, the Schwarz-Christoffel mapping problem can be solved analytically in terms of elliptic integrals whose values can be conveniently found in tables. Unfortunately, when the geometry of the conductor-dielectric system becomes complex, the Schwarz-Christoffel mapping problem can no longer be solved analytically. This becomes the case when the conductors have *finite thickness*. The fringing effects of the thickness should be taken into consideration in order to accurately estimate the delay of the metallic lines in VLSI circuits [5].

The practical implementation of this technique thus requires *numerical* solution of the Schwarz-Christoffel problem, which has only recently become feasible for general polygons [6]. A Fortran package for Schwarz-Christoffel mapping problems, called the SCPACK, has been designed by Trefethen, and is available for public use from its author [7]. The SCPACK first finds a map between the w plane and the unit circle, and then maps the points on the unit circle to the points on the z plane. This two-level mapping technique allows the program to deal with more general polygons.

We have applied the SCPACK to various interconnection geometries. Fig. 2 illustrates integration paths of some of these interconnection structures. The computations were performed on a VAX-11/780 running UNIX 4.3 BSD using single precision. The computation of the ratio L/d takes less than 30 s for the problems we have tried. The results are summarized in Table I.

For these geometries, we have also computed the capacitance using an interactive program which implements the *segmentation method* explained in [3]. In this method, each conductor surface is replaced by a number of small rectangular segments, permitting the establishment of a linear relationship between potentials assigned to the conductor segments and their unknown charges. The capacitance of each geometry is then computed by solving a set of linear equations. These results are also given in Table I. Using the Schwarz-Christoffel mapping technique, we therefore were able to validate some of the results produced by the segmentation method which deals with more general geometries than those given in Fig. 2.

The capacitance values computed by the Schwarz-Christoffel technique can be used to calibrate simulators designed for more general applications. Such calibration process is very useful; for example for a specified accuracy, the necessary number of segments in the segmentation method may be determined. This relates to the computer time and computer resources required for running simulation problems.

The SCPACK can also be used for field plotting, even though it employs excessive machinery to perform the computations. The field plotting is achieved by mapping a rectilinear grid in Fig. 1(d) back to Fig. 1(a). This involves the computation of the maps $z = g^{-1}(w)$ from Fig. 1(d) to Fig. 1(c), and $w = f(z)$ from Fig. 1(b) to Fig. 1(a). The evaluation of the inverse map is accomplished by

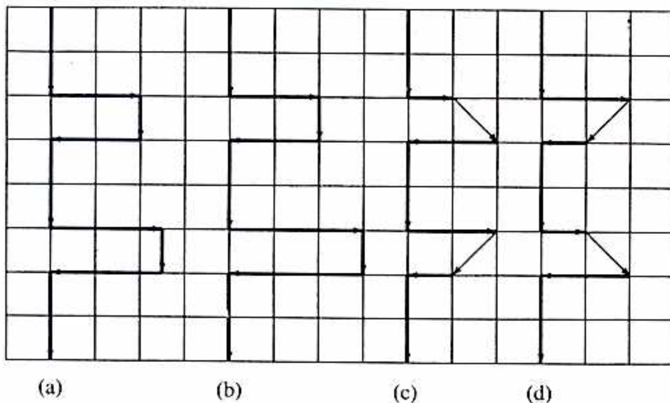

Fig. 2. Integration paths for different conductor–dielectric geometries.

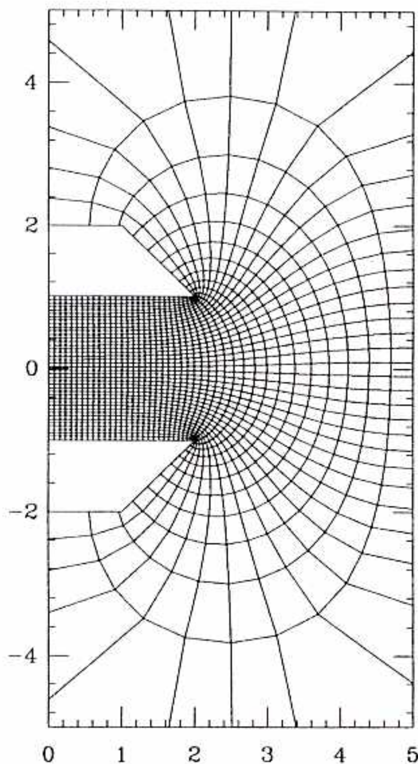

Fig. 3. Equipotential and streamlines for Fig. 2(c).

TABLE I
THE CAPACITANCE PER UNIT LENGTH (F/m) BY SCHWARZ–CHRISTOFFEL AND SEGMENTATION METHODS

	Schwarz-Christoffel		Segmentation
Geometry	L/d	Capacitance	Capacitance
Fig. 2(a)	0.613321	1.085578×10^{-11}	1.09×10^{-11}
Fig. 2(b)	0.557196	9.862369×10^{-12}	9.86×10^{-12}
Fig. 2(c)	0.637115	1.127694×10^{-11}	1.13×10^{-11}
Fig. 2(d)	0.736467	1.303547×10^{-11}	1.31×10^{-11}

first using an ODE solver to generate an initial estimate, which is then improved upon by Newton's method. The computation of the forward map utilizes compound Gauss–Jacobi quadrature. Obviously these computations can be performed more directly by evaluating elliptic functions and elliptic integrals. Nevertheless, the techniques of the SCPACK produce somewhat more reliable results [6]. Fig. 3 shows the equipotential and the streamlines for the geometry given in Fig. 2(c). This computation requires longer CPU time, usually on the order of minutes.

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An Accurate and Efficient Delay Time Modeling for MOS Logic Circuits Using Polynomial Approximation

YOUNG-HYUN JUN, KI JUN, AND SONG-BAI PARK, MEMBER, IEEE

***Abstract*—A new delay model is proposed for multiple delay simulation for NMOS and CMOS logic circuits. For the simple inverter the rise or fall delay time is approximated by a product of polynomials of the input waveform slope, the output loading capacitance, and the device configuration ratio, with the polynomial coefficients determined so as to best fit the SPICE simulation results for a given fabrication process. This approach can easily be extended to the case of multiple-input transitions. The simulation results show that the proposed model can predict the delay times within 5 percent error and with a speedup of three orders of magnitude for several circuits tested as compared with the SPICE simulation.**

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The authors are with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, P.O. Box 150, Cheongyang, Seoul, Korea.

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